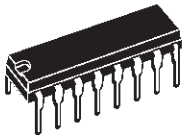
HCF4510B
HCF4516B

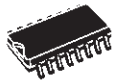
PRESETTABLE UP/DOWN COUNTERS

- MEDIUM SPEED OPERATION f_{CL} = 8MHz TYP. AT 10V
- SYNCHRONOUS INTERNAL CARRY PROPAGATION
- RESET AND PRESET CAPABILITY
- QUIESCENT CURRENT SPECIFIED TO 15V
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 15V AND 25°C
- 100% TESTED FOR QUIESCENT CURRENT

MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



DIP



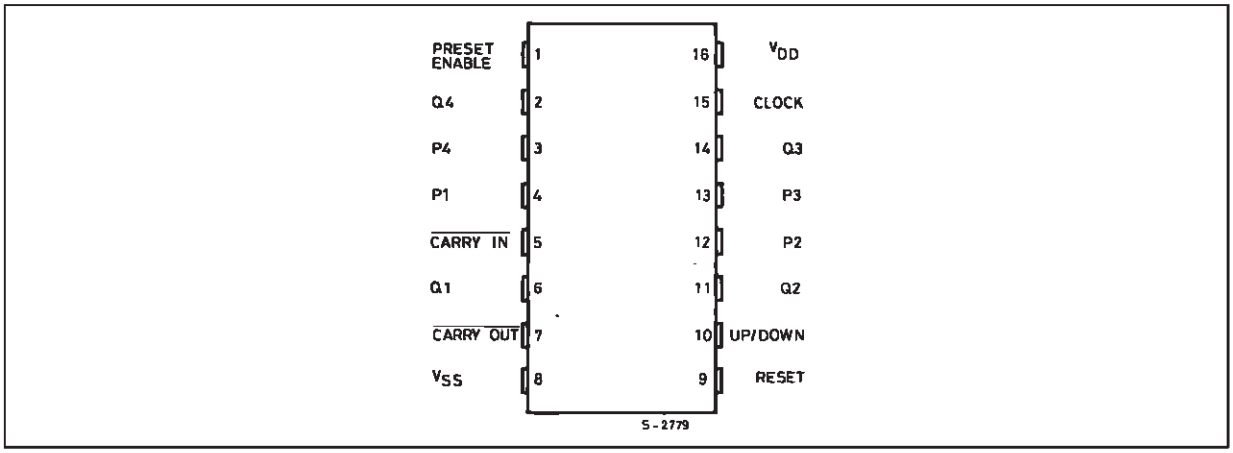
SOP

ORDER CODES		
PACKAGE	**TUBE**	**T & R**
DIP	HCF45XXBEY	
SOP	HCF45XXBM1	HCF45XXM013TR

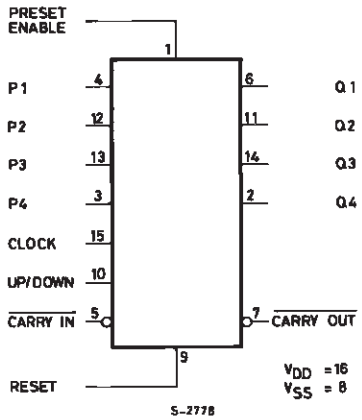
DESCRIPTION

The HCF4510B and HCF4516B are monolithic integrated circuits available in 16-lead dual in-line plastic and plastic micro package. The HCF4510B Presettable BCD Up/Down Counter and the HCF4516B Presettable Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The HCF4510B will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode. If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage. The HCF4510B and HCF4516B can be loaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage.

PIN CONNECTION



FUNCTIONAL DIAGRAM



TRUTH TABLE

CL	CI	U/D	PE	R	Action
X	1	X	0	0	No Count
⎍	0	1	0	0	Count Up
⎍	0	0	0	0	Count Down
X	X	X	1	0	Preset
X	X	X	X	1	Reset

X= Don't care

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DD} *	Supply Voltage	-0.5 to +18	V
V_i	Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for Top = Full Package Temperature Range	200 100	mW mW
T_{op}	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

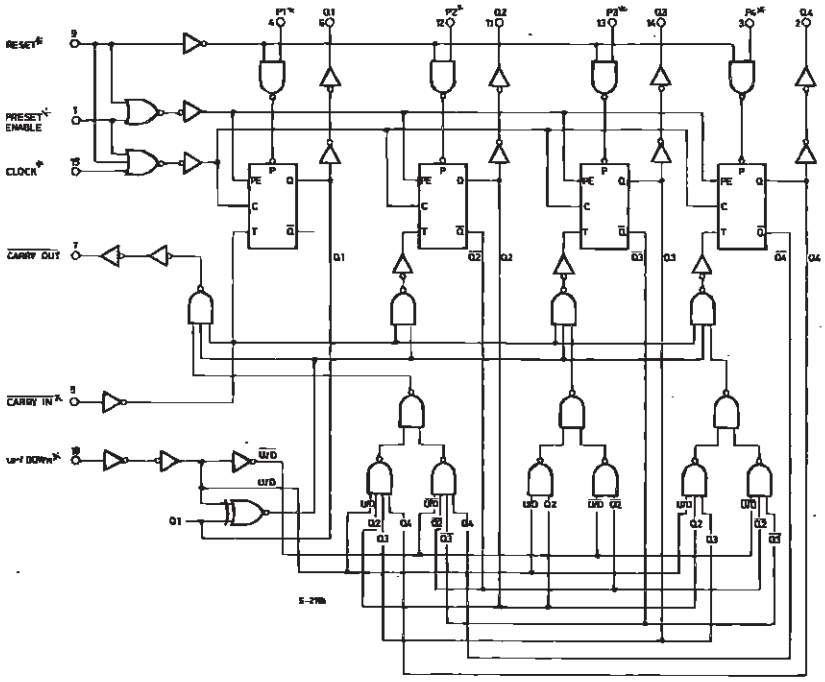
* All voltage values are referred to V_{SS} pin voltage.

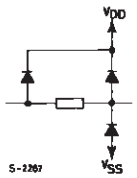
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 15	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-40 to +85	°C

LOGIC DIAGRAMS

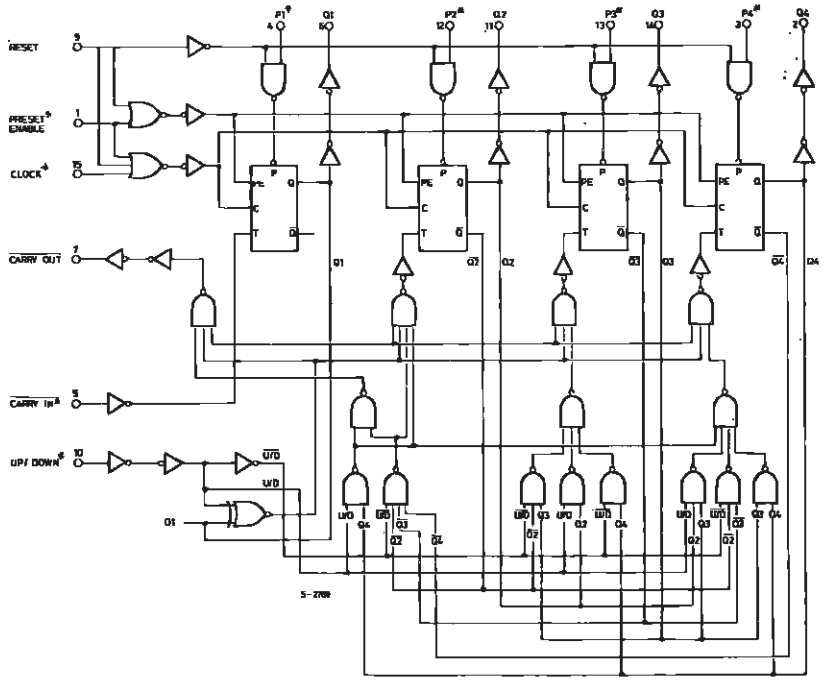
4510B

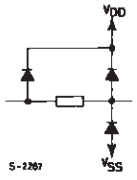




ALL INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

4516B

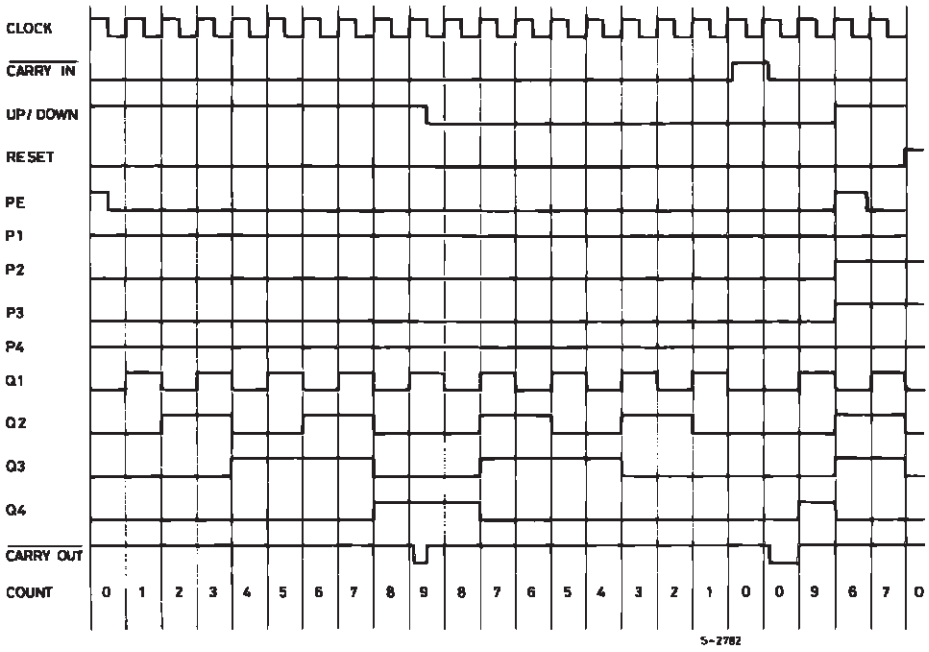




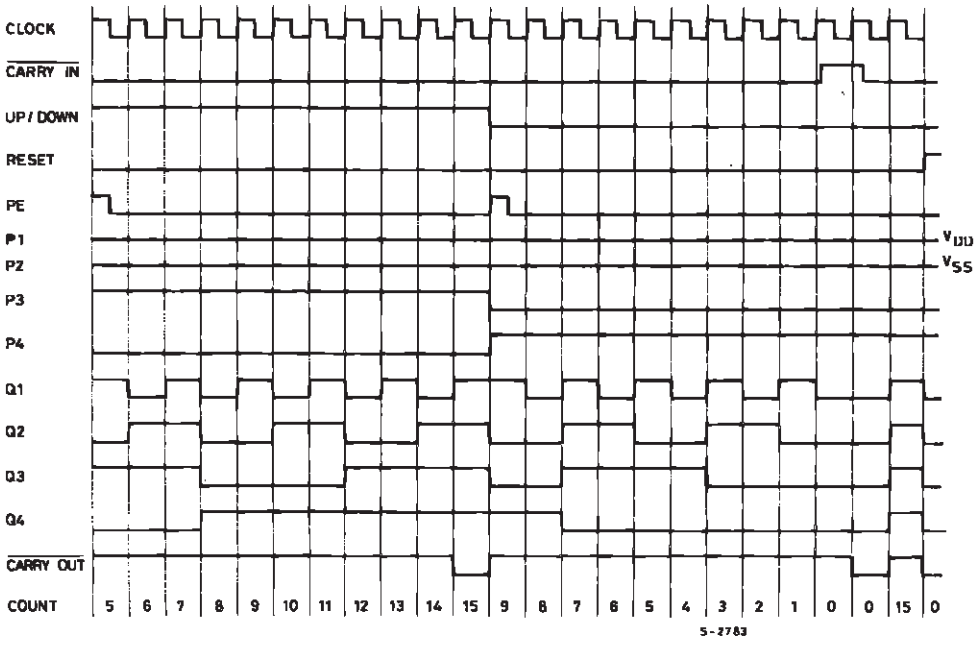
ALL INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

TIMING DIAGRAMS

4510B



4516B



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter	Test Conditios				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	-40 °C		25 °C			85 °C		
						Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		20		0.02	20		150	μA
		0/10			10		40		0.02	40		300	
		0/15			15		80		0.02	80		600	
V_{OH}	Output High Voltage	0/5		< 1	5	4.95		4.95			4.95		V
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage	5/0		< 1	5		0.05			0.05		0.05	V
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current	0/5	2.5		5	-1.53		-1.36	-3.2		-1.1		mA
		0/5	4.6		5	-0.52		-0.44	-1		-0.36		
		0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
		0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output Sink Current	0/5	0.4		5	0.52		0.44	1		0.36		mA
		0/10	0.5		10	1.3		1.1	2.6		0.9		
		0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	0/15	Any Input		15		±0.3		$±10^{-5}$	±0.3		±1	μA
C_I	Input Capacitance		Any Input						5	7.5			pF

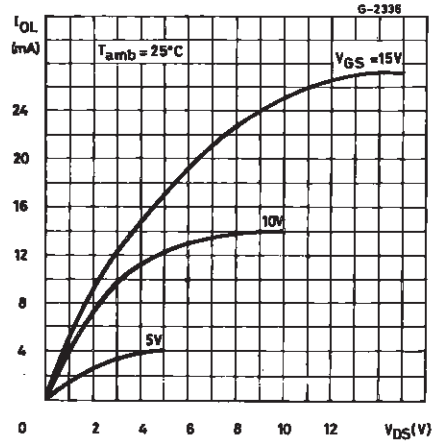
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5 V, 2 V min. with V_{DD} = 10 V, 2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, C_L = 50 pF, R_L = 200 KΩ, typical temperature coefficent for all V_{DD} values is 03 %/°C, all input rise and fall times= 20 ns)

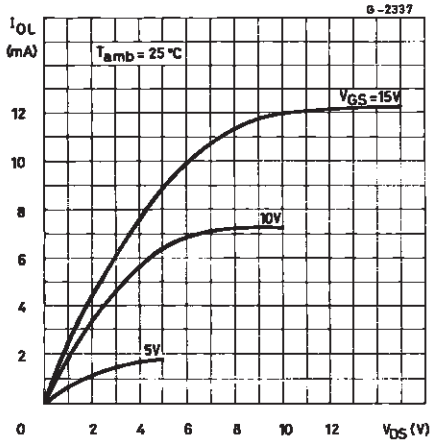
Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time Clock to Q Output		5		200	400	ns
			10		100	200	
			15		75	150	
t_{PHL} t_{PLH}	Propagation Delay Time Preset or Reset to Q Output		5		210	420	ns
			10		105	210	
			15		80	160	
t_{PHL} t_{PLH}	Propagation Delay Time Clock to Carry Out		5		240	480	ns
			10		120	240	
			15		90	180	
t_{PHL} t_{PLH}	Propagation Delay Time Carry In to Carry Out		5		125	250	ns
			10		60	120	
			15		50	100	
t_{PHL} t_{PLH}	Propagation Delay Time Preset or Reset to Carry Out		5		320	640	ns
			10		160	320	
			15		125	250	
t_{THL} t_{TLH}	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
f_{MAX}	Max Clock Frequency		5	2	4		MHz
			10	4	8		
			15	5.5	11		
t_W	Clock Pulse Width		5	150			ns
			10	75			
			15	60			
	Preset Enable or Reset Removal Time (1)		5	150			ns
			10	80			
			15	60			
t_r, t_f	Clock Rise and Fall Time (2)		5			15	µs
			10			5	
			15			5	
t_{setup}	Carry In Setup Time		5	130			ns
			10	60			
			15	45			
t_{setup}	Up Down Setup Time		5	360			ns
			10	160			
			15	110			
t_W	Preset Enable or Reset Pulse Width		5	220			ns
			10	100			
			15	75			

(1) Time required after the falling edge of the reset or preset enable inuts before the rising edge of the clock will trigger the counter (similar to setup time).
(2) If more than unit is cascated in the parallel clocked application, trCL should be made less than or equal to the sum of the fixed propagation delay at 15pF and the transition time of the carry output driving stage of the estimated capacitive load.

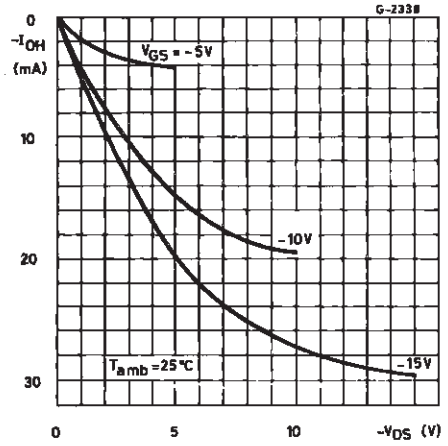
Typical Output Low (sink) Current Characteristics.



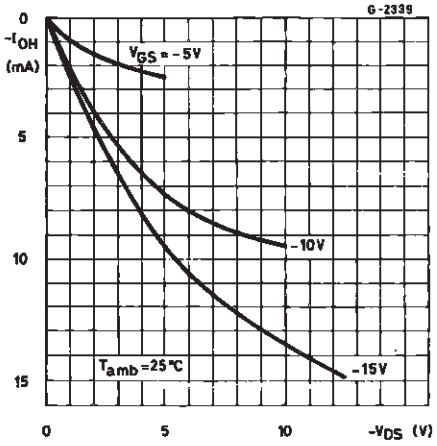
Minimum Output Low (sink) Current Characteristics.



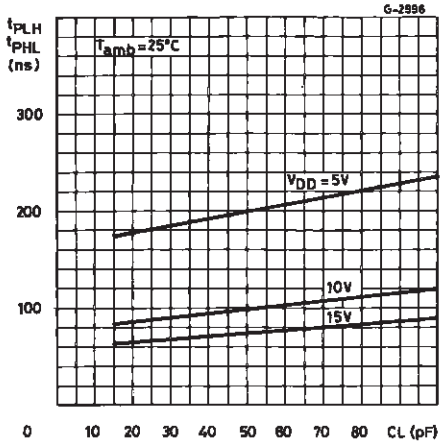
Typical Output High (source) Current Characteristics.



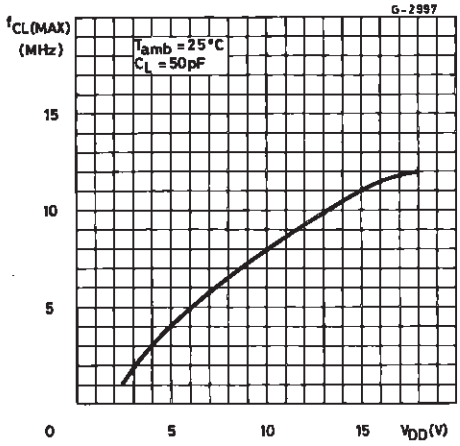
Minimum Output High (source) Current Characteristics.



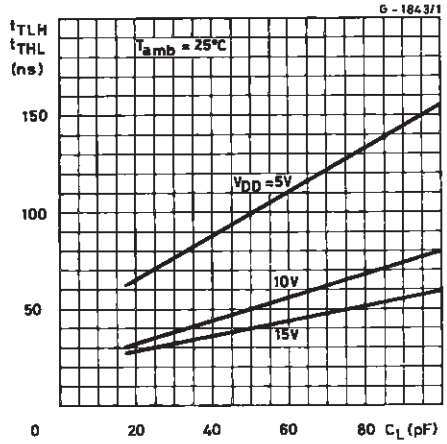
Typical Propagation Delay Time vs. Load Capacitance for Clock to Q Output.



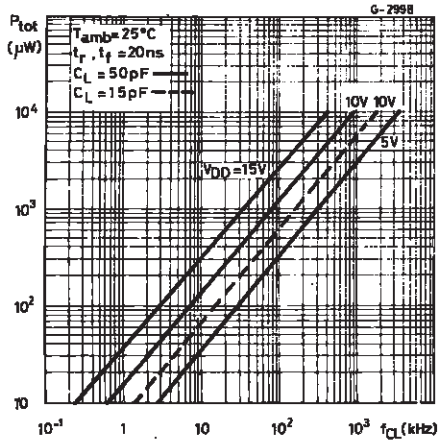
Typical Maximum Clock Input Frequency vs. Supply Voltage.



Typical Transition Time vs. Load Capacitance.

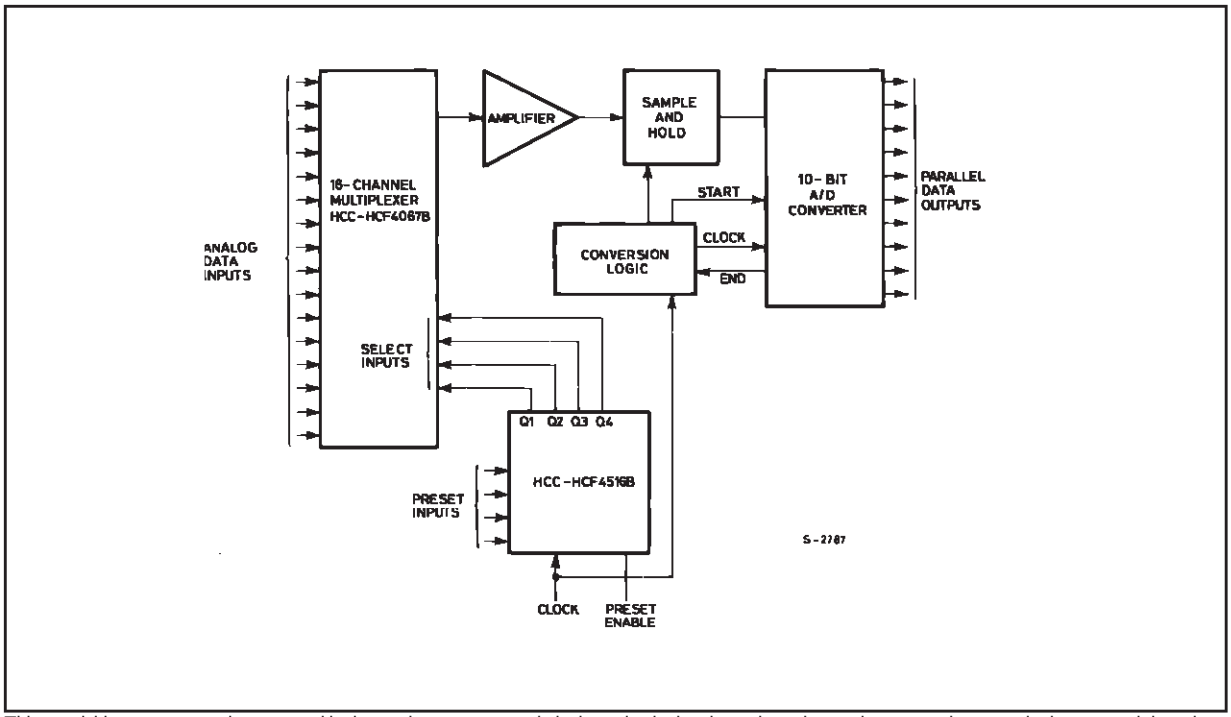


Typical Dynamic Power Dissipation vs. Frequency.



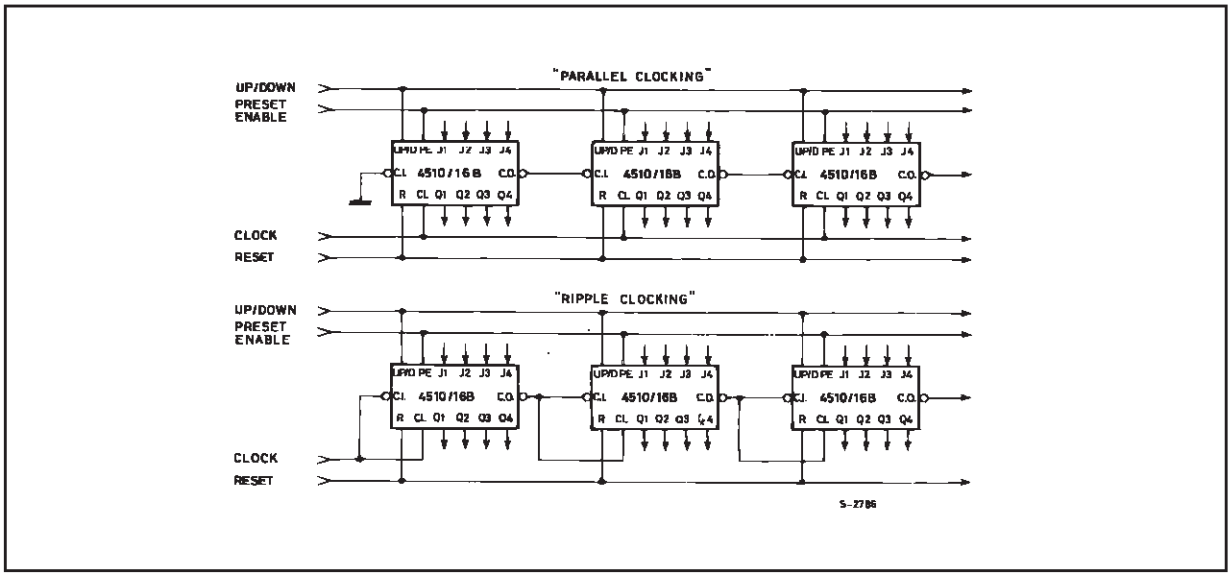
TYPICAL APPLICATIONS

TYPICAL 16-CHANNEL, 10 BIT DATA ACQUISITION SYSTEM



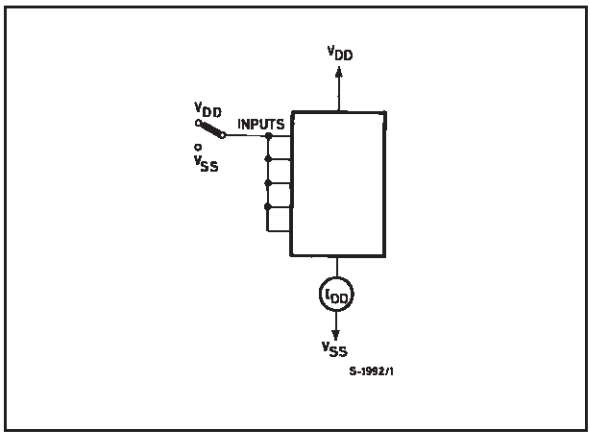
This acquisition system can be operated in the random access mode by jamming in the channel number at the present inputs, or in the sequential mode by clocking the HCF4516B.

CASCADING COUNTER PACKAGES

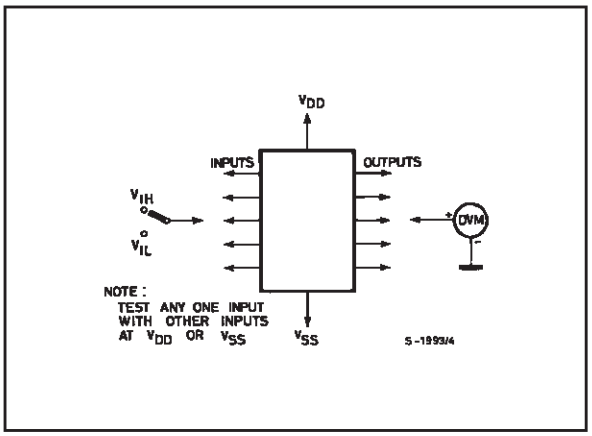


TEST CIRCUITS

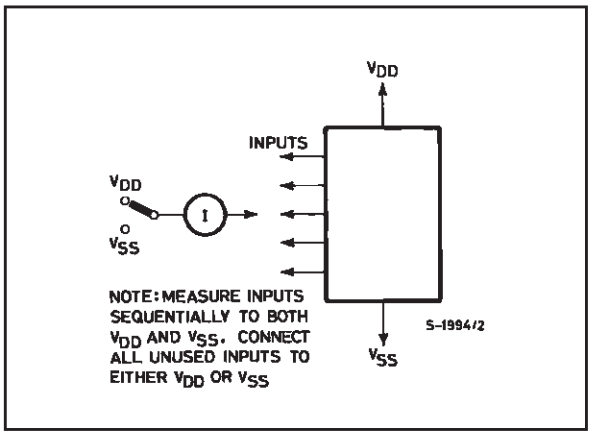
Quiescent Device Current.



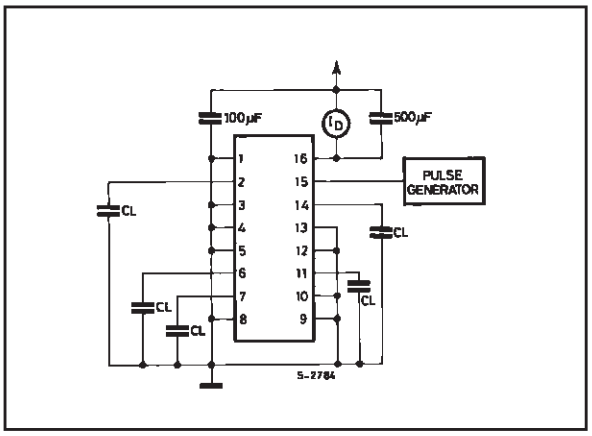
Noise Immunity.



Input Leakage Current.

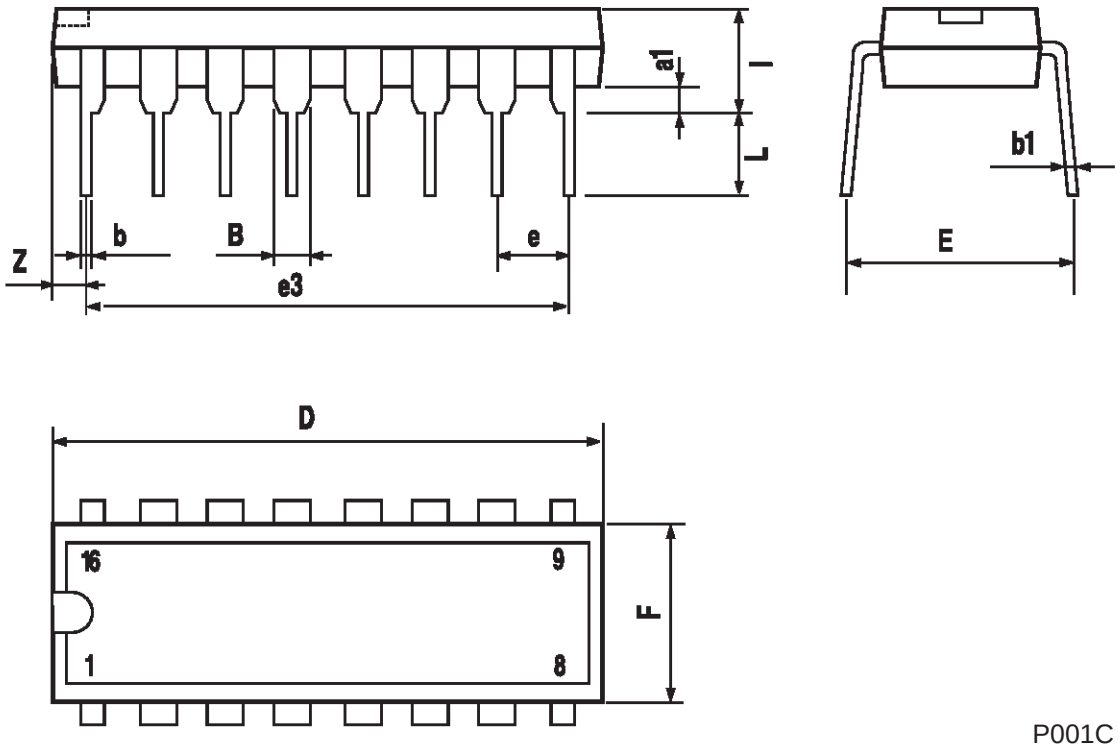


Power Dissipation and Input Waveform.



Plastic DIP-16 (0.25) MECHANICAL DATA

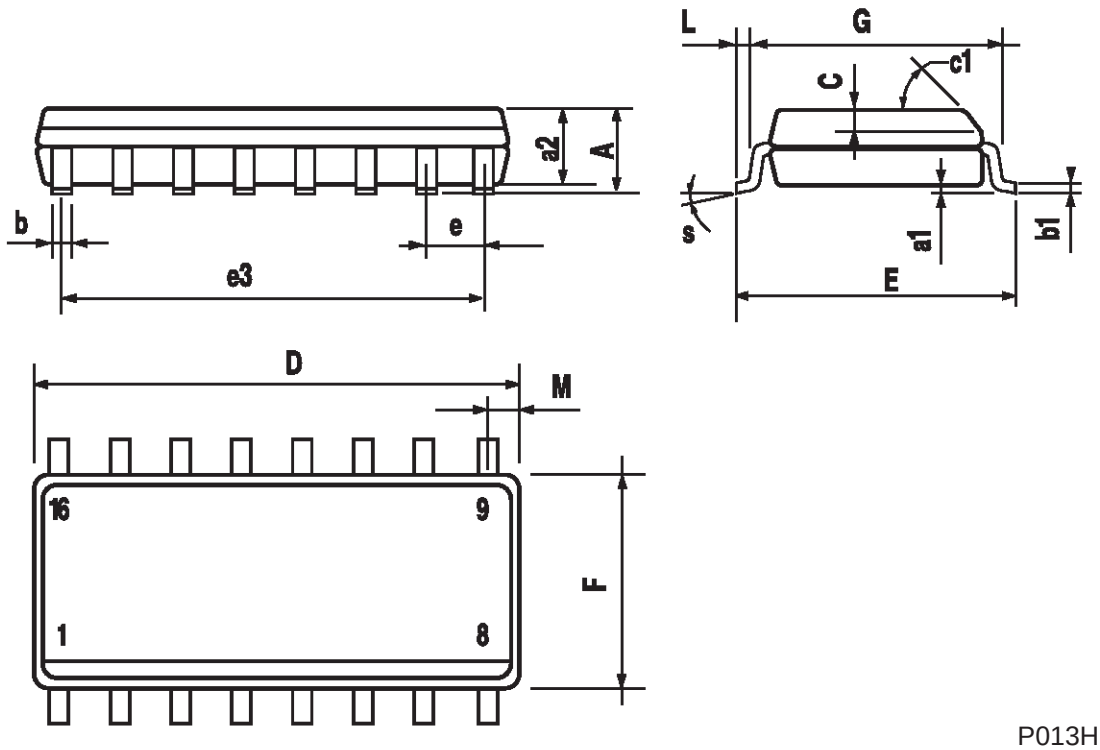
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					



P013H

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