HARRIS Semiconductor

# HD-6402

## CMOS Universal Asynchronous Receiver Transmitter (UART)

March 1997

### Features

- **8.0MHz Operating Frequency (HD-6402B)**
- **2.0MHz Operating Frequency (HD-6402R)**
- **Low Power CMOS Design**
- **Programmable Word Length, Stop Bits and Parity**
- **Automatic Data Formatting and Status Generation**
- **Compatible with Industry Standard UARTs**
- **Single +5V Power Supply**
- **CMOS/TTL Compatible Inputs**

### Description

The HD-6402 is a CMOS UART for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5-bit code.

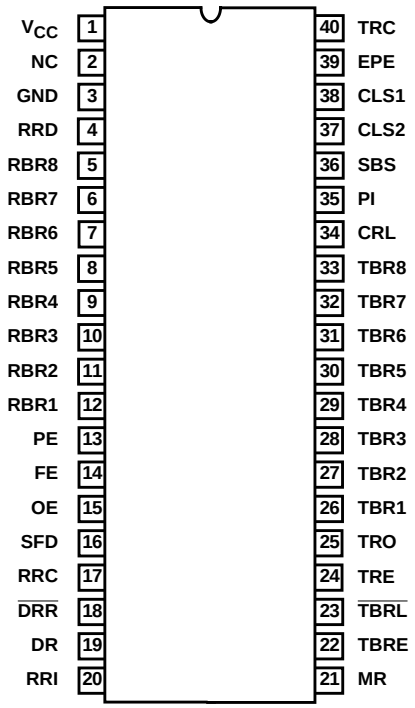
The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. Utilizing the Harris advanced scaled SAJI IV CMOS process permits operation clock frequencies up to 8.0MHz (500K Baud). Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

### Ordering Information

| PACKAGE | TEMPERATURE RANGE | 2MHz = 125K BAUD | 8MHz = 500K BAUD | PKG. NO. |
|---|---|---|---|---|
| Plastic DIP | -40$^{o}$C to +85$^{o}$C | HD3-6402R-9 | HD3-6402B-9 | E40.6 |
| CERDIP | -40$^{o}$C to +85$^{o}$C | HD1-6402R-9 | HD1-6402B-9 | F40.6 |
| SMD# | -55$^{o}$C to +125$^{o}$C | 5962-9052501MQA | 5962-9052502MQA | F40.6 |

### Pinout

**HD-6402 (PDIP, CERDIP)**
TOP VIEW

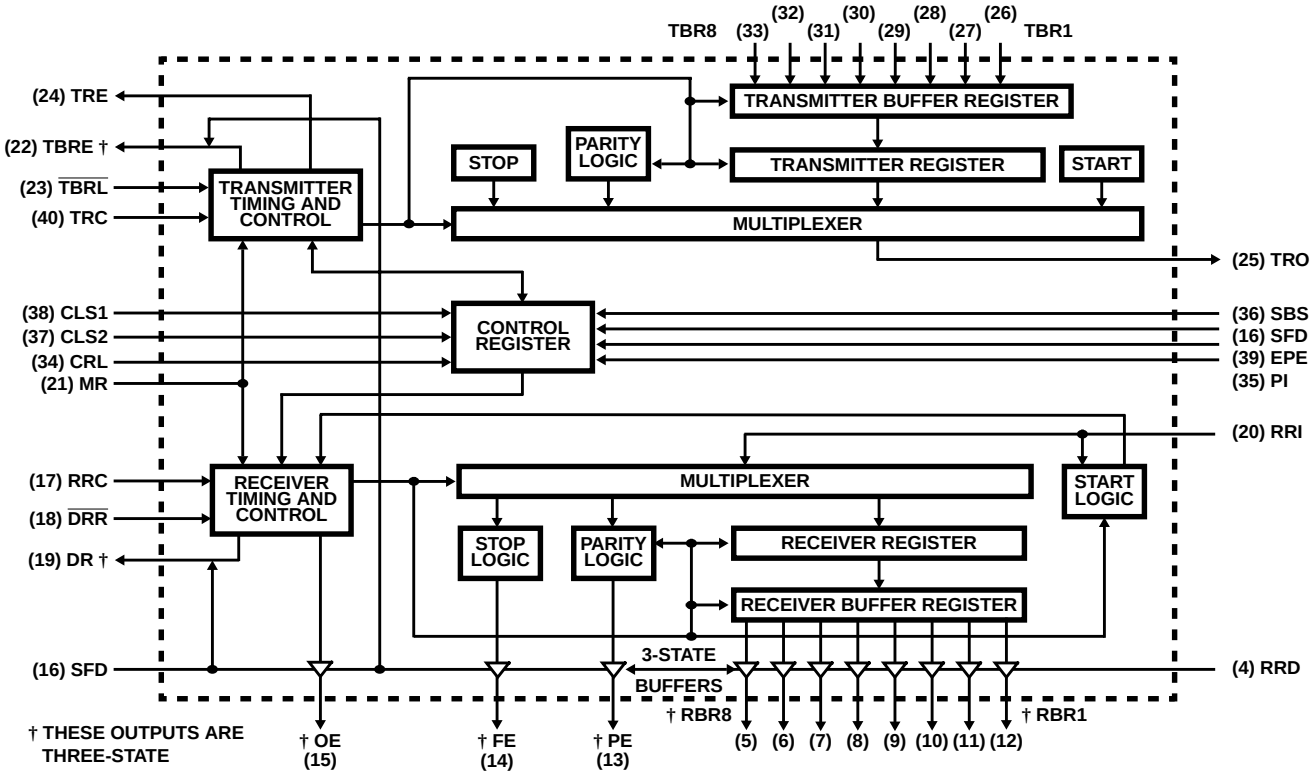



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.



File Number **2956.1**

## Functional Diagram



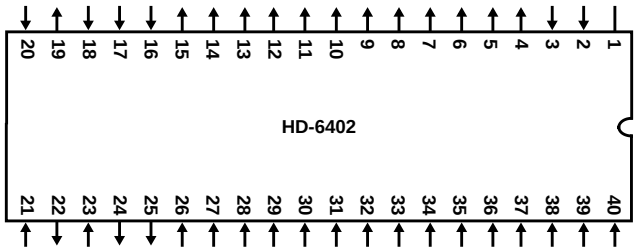

## Control Definition

| CONTROL WORD | | | | | CHARACTER FORMAT | | | |
|---|---|---|---|---|---|---|---|---|
| CLS 2 | CLS 1 | PI | EPE | SBS | START BIT | DATA BITS | PARITY BIT | STOP BITS |
| 0 | 0 | 0 | 0 | 0 | 1 | 5 | ODD | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 5 | ODD | 1.5 |
| 0 | 0 | 0 | 1 | 0 | 1 | 5 | EVEN | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 5 | EVEN | 1.5 |
| 0 | 0 | 1 | X | 0 | 1 | 5 | NONE | 1 |
| 0 | 0 | 1 | X | 1 | 1 | 5 | NONE | 1.5 |
| 0 | 1 | 0 | 0 | 0 | 1 | 6 | ODD | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 6 | ODD | 2 |
| 0 | 1 | 0 | 1 | 0 | 1 | 6 | EVEN | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 6 | EVEN | 2 |
| 0 | 1 | 1 | X | 0 | 1 | 6 | NONE | 1 |
| 0 | 1 | 1 | x | 1 | 1 | 6 | NONE | 2 |
| 1 | 0 | 0 | 0 | 0 | 1 | 7 | ODD | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 7 | ODD | 2 |
| 1 | 0 | 0 | 1 | 0 | 1 | 7 | EVEN | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 7 | EVEN | 2 |
| 1 | 0 | 1 | X | 0 | 1 | 7 | NONE | 1 |
| 1 | 0 | 1 | x | 1 | 1 | 7 | NONE | 2 |
| 1 | 1 | 0 | 0 | 0 | 1 | 8 | ODD | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 8 | ODD | 2 |
| 1 | 1 | 0 | 1 | 0 | 1 | 8 | EVEN | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 8 | EVEN | 2 |
| 1 | 1 | 1 | X | 0 | 1 | 8 | NONE | 1 |
| 1 | 1 | 1 | x | 1 | 1 | 8 | NONE | 2 |

## Pin Description

| PIN | TYPE | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 1 | | $V_{CC}$ † | Positive Voltage Supply |
| 2 | | NC | No Connection |
| 3 | | GND | Ground |
| 4 | I | RRD | A high level on RECEIVER REGISTER DISABLE forces the receiver holding out-puts RBR1-RBR8 to high impedance state. |
| 5 | O | RBR8 | The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1. |
| 6 | O | RBR7 | See Pin 5-RBR8 |
| 7 | O | RBR6 | See Pin 5-RBR8 |
| 8 | O | RBR5 | See Pin 5-RBR8 |
| 9 | O | RBR4 | See Pin 5-RBR8 |
| 10 | O | RBR3 | See Pin 5-RBR8 |
| 11 | O | RBR2 | See Pin 5-RBR8 |
| 12 | O | RBR1 | See Pin 5-RBR8 |
| 13 | O | PE | A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low. |
| 14 | O | FE | A high level on FRAMING ERROR indicates the first stop bit was invalid. |
| 15 | O | OE | A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. |
| 16 | I | SFD | A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state. |
| 17 | I | RRC | The Receiver register clock is 16X the receiver data rate. |
| 18 | I | $\overline{DRR}$ | A low level on DATA RECEIVED RESET clears the data received output DR to a low level. |
| 19 | O | DR | A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register. |
| 20 | I | RRI | Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register. |
| 21 | I | MR | A high level on MASTER RESET clears PE, FE, OE and DR to a low level and sets the transmitter register empty (TRE) to a high level 18 clock cycles after MR falling edge. MR does not clear the receiver buffer register. This input must be pulsed at least once after power up. The HD-6402 must be master reset after power up. The reset pulse should meet $V_{IH}$ and $t_{MR}$. Wait 18 clock cycles after the falling edge of MR before beginning operation. |
| 22 | O | TBRE | A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data. |
| 23 | I | $\overline{TBRL}$ | A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ initiates data transfer to the transmitter register. If busy, transfer is automatically delayed so that the two characters are transmitted end to end. |
| 24 | O | TRE | A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits. |
| 25 | O | TRO | Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT. |
| 26 | I | TRB1 | Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8 bits the TBR8, 7 and 6 inputs are ignored corresponding to their programmed word length. |
| 27 | I | TBR2 | See Pin 26-TBR1. |
| 28 | I | TBR3 | See Pin 26-TBR1. |
| 29 | I | TBR4 | See Pin 26-TBR1. |
| 30 | I | TBR5 | See Pin 26-TBR1. |
| 31 | I | TBR6 | See Pin 26-TBR1. |
| 32 | I | TBR7 | See Pin 26-TBR1. |
| 33 | I | TBR8 | See Pin 26-TBR1. |
| 34 | I | CRL | A high level on CONTROL REGISTER LOAD loads the control register with the control word. The control word is latched on the falling edge of CRL. CRL may be tied high. |
| 35 | I | PI | A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low. |
| 36 | I | SBS | A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths. |
| 37 | I | CLS2 | These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits.) |
| 38 | I | CLS1 | See Pin 37-CLS2. |
| 39 | I | EPE | When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity. |
| 40 | I | TRC | The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate. |

† A 0.1µF decoupling capacitor from the $V_{CC}$ pin to the GND is recommended.



## Transmitter Operation

The transmitter section accepts parallel data, formats the data and transmits the data in serial form on the Transmitter Register Output (TRO) terminal (See serial data format). Data is loaded from the inputs TBR1-TBR8 into the Transmitter Buffer Register by applying a logic low on the Transmitter Buffer Register Load ($\overline{TBRL}$) input (A). Valid data must be present at least $t_{set}$ prior to and $t_{hold}$ following the rising edge of $\overline{TBRL}$. If words less than 8 bits are used, only the least significant bits are transmitted. The character is right justified, so the least significant bit corresponds to TBR1 (B).

The rising edge of $\overline{TBRL}$ clears Transmitter Buffer Register Empty (TBRE). 0 to 1 Clock cycles later, data is transferred to the transmitter register, the Transmitter Register Empty (TRE) pin goes to a low state, TBRE is set high and serial data information is transmitted. The output data is clocked by Transmitter Register Clock (TRC) at a clock rate 16 times the data rate. A second low level pulse on $\overline{TBRL}$ loads data into the Transmitter Buffer Register (C). Data transfer to the transmitter register is delayed until transmission of the current data is complete (D). Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.

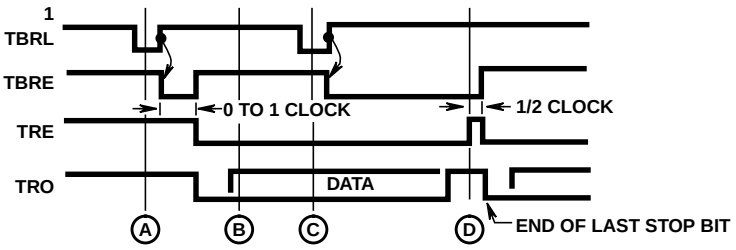



**FIGURE 1. TRANSMITTER TIMING (NOT TO SCALE)**

## Receiver Operation

Data is received in serial form at the Receiver Register Input (RRI). When no data is being received, RRI must remain high. The data is clocked through the Receiver Register Clock (RRC). The clock rate is 16 times the data rate. A low level on Data Received Reset ($\overline{DRR}$) clears the Data Receiver (DR) line (A). During the first stop bit data is transferred from the Receiver Register to the Receiver Buffer Register (RBR) (B). If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on Overrun Error (OE) indicates overruns. An overrun occurs when DR has not been cleared before the present character was transferred to the RBR. One clock cycle later DR is reset to a logic high, and Framing Error (FE) is evaluated (C). A logic high on FE indicates an invalid stop bit was received, a framing error. A logic high on Parity Error (PE) indicates a parity error.

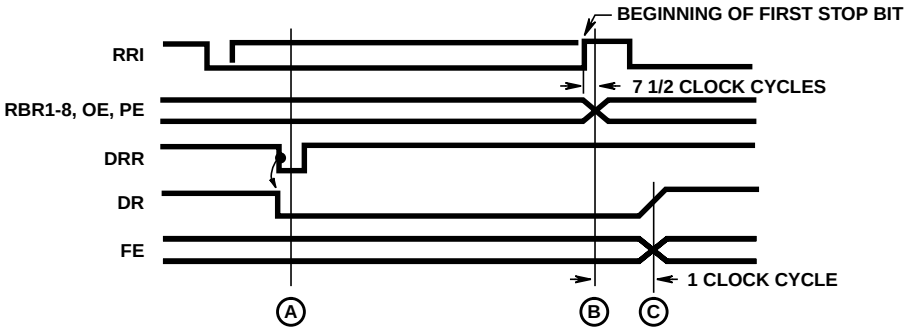



**FIGURE 2. RECEIVER TIMING (NOT TO SCALE)**

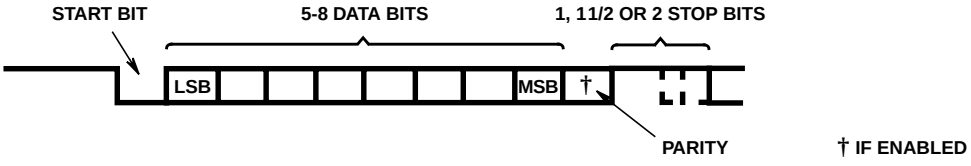



**FIGURE 3. SERIAL DATA FORMAT**

## Start Bit Detection

The receiver uses a 16X clock timing. The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion (A). The center of the start bit is defined as clock count 7 1/2. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle, ±1/32 bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.

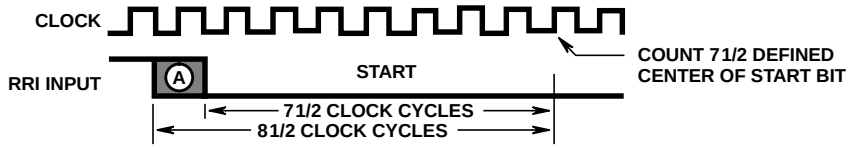



**FIGURE 4.**

## Interfacing with the HD-6402

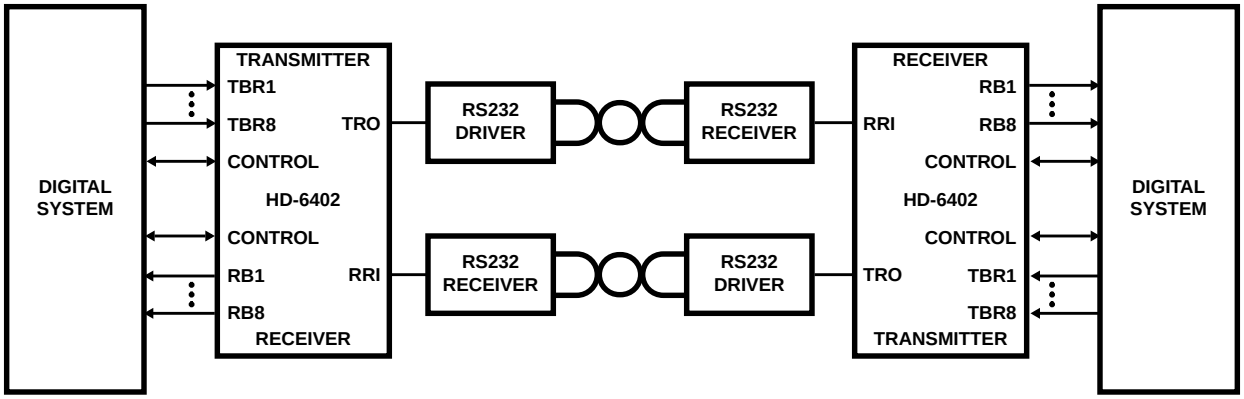



**FIGURE 5. TYPICAL SERIAL DATA LINK**

## Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied . . . . . GND -0.5V to $V_{CC}$ +0.5V
Storage Temperature Range . . . . . $-65^oC$ to $+150^oC$
Junction Temperature . . . . . $+175^oC$
Lead Temperature (Soldering 10s) . . . . . $+300^oC$
ESD Classification . . . . . Class 1
Typical Derating Factor . . . . . 1mA/MHz Increase in ICCOP

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ | $\theta_{JC}$ |
|---|---|---|
| CERDIP Package | $50^oC/W$ | $12^oC/W$ |
| PDIP Package | $50^oC/W$ | N/A |

Gate Count . . . . . 1643 Gates

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V

Operating Temperature Range
HD-6402R-9, HD6402B-9 . . . . . $-40^oC$ to $+85^oC$

## DC Electrical Specifications $V_{CC} = 5.0V \pm 10\%$, $T_A = -40^oC$ to $+85^oC$ (HD-6402R-9, HD-6402B-9)

| SYMBOL | PARAMETER | LIMITS MIN | LIMITS MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| $V_{IH}$ | Logical "1" Input Voltage | 2.0 | - | V | $V_{CC}$ = 5.5V |
| $V_{IL}$ | Logical "0" Input Voltage | - | 0.8 | V | $V_{CC}$ = 4.5V |
| II | Input Leakage Current | -1.0 | 1.0 | µA | $V_{IN}$ = GND or $V_{CC}$, $V_{CC}$ = 5.5V |
| $V_{OH}$ | Logical "1" Output Voltage | 3.0<br>$V_{CC}$ -0.4 | -<br>- | V | $I_{OH}$ = -2.5mA, $V_{CC}$ = 4.5V<br>$I_{OH}$ = -100µA |
| $V_{OL}$ | Logical "0" Output Voltage | - | 0.4 | V | $I_{OL}$ = +2.5mA, $V_{CC}$ = 4.5V |
| $I_O$ | Output Leakage Current | -1.0 | 1.0 | µA | $V_O$ = GND or $V_{CC}$, $V_{CC}$ = 5.5V |
| ICCSB | Standby Supply Current | - | 100 | µA | $V_{IN}$ = GND or $V_{CC}$; $V_{CC}$ = 5.5V, Output Open |
| ICCOP | Operating Supply Current (See Note) | - | 2.0 | mA | $V_{CC}$ = 5.5V, Clock Freq. = 2MHz, $V_{IN}$ = $V_{CC}$ or GND, Outputs Open |

NOTE: Guaranteed, but not 100% tested

## Capacitance $T_A = +25^oC$

| PARAMETER | SYMBOL | CONDITIONS | LIMIT TYPICAL | UNITS |
|---|---|---|---|---|
| Input Capacitance | CIN | Freq. = 1MHz, all measurements are referenced to device GND | 25 | pF |
| Output Capacitance | COUT | | 25 | pF |

## AC Electrical Specifications $V_{CC} = 5.0V \pm 10\%$, $T_A = -40^oC$ to $+85^oC$ (HD-6402R-9, HD6402B-9)

| SYMBOL | PARAMETER | LIMITS HD-6402R MIN | LIMITS HD-6402R MAX | LIMITS HD-6402B MIN | LIMITS HD-6402B MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|
| (1) fCLOCK | Clock Frequency | D.C. | 2.0 | D.C. | 8.0 | MHz | $C_L$ = 50pF<br>See Switching Waveform |
| (2) $t_{PW}$ | Pulse Widths, CRL, DRR, TBRL | 150 | - | 75 | - | ns | |
| (3) $t_{MR}$ | Pulse Width MR | 150 | - | 150 | - | ns | |
| (4) $t_{SET}$ | Input Data Setup Time | 50 | - | 20 | - | ns | |
| (5) $t_{HOLD}$ | Input Data Hold Time | 60 | - | 20 | - | ns | |
| (6) $t_{EN}$ | Output Enable Time | - | 160 | - | 35 | ns | |

## Switching Waveforms

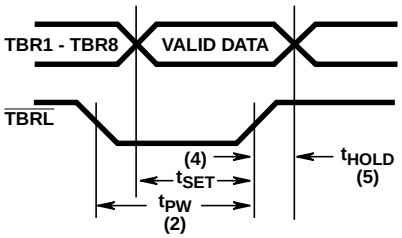



FIGURE 6. DATA INPUT CYCLE

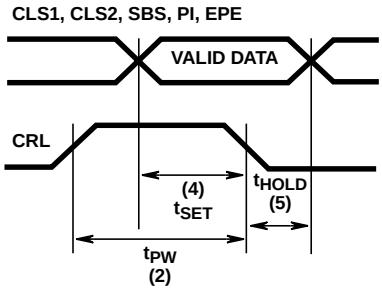



FIGURE 7. CONTROL REGISTER LOAD CYCLE

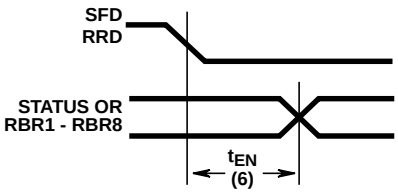



FIGURE 8. STATUS FLAG OUTPUT ENABLE TIME OR DATA OUTPUT ENABLE TIME

## A.C. Testing Input, Output Waveform

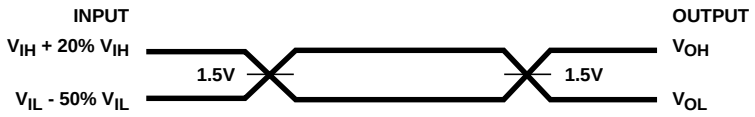



FIGURE 9.

NOTE: A.C. Testing: All input signals must switch between $V_{IL}$ - 50% $V_{IL}$ and $V_{IH}$ + 20% $V_{IH}$. Input rise and fall times are driven at 1ns/V.

## Test Circuit

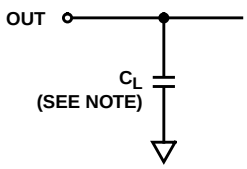



FIGURE 10.

NOTE: Includes stray and jig capacitance, $C_L$ = 50pF.